What is claimed is:

1. A method comprising:

receiving a data sequence in a receiver having a plurality of lanes;

detecting a predetermined character in the data sequence in a first lane; and

tracking a time period until the predetermined character is detected in the plurality of lanes.

2. The method of claim 1, further comprising resetting the receiver if a predetermined number of cycles is exceeded before the predetermined character is detected in the plurality of lanes.

3. The method of claim 1, further comprising realigning the data sequence based on when the predetermined character is detected in each of the plurality of lanes.

4. The method of claim 3, further comprising transmitting the realigned data sequence from the receiver after the predetermined character is detected in the plurality of lanes.

5. The method of claim 3, further comprising determining whether the predetermined character is received simultaneously on the plurality of lanes.

6. The method of claim 1, wherein the data sequence comprises a training sequence.

7. The method of claim 1, wherein the data sequence is byte striped.

8. A method comprising:

receiving data packets on a plurality of channels of a receiver;

determining whether the data packets are misaligned while the data packets are maintained in buffers corresponding to the plurality of channels; and

aligning the data packets if the data packets are misaligned.

9. The method of claim 8, wherein determining whether the data packets are misaligned comprises analyzing whether a predetermined value is received on each of the plurality of channels within a first time period.

10. The method of claim 8, further comprising transmitting the data packets in an aligned manner.

11. The method of claim 10, further comprising holding the data packets until each of the buffers has a predefined depth.

12. The method of claim 8, further comprising realigning the data packets if the data packets become misaligned.

13. The method of claim 8, wherein the data packets are byte striped.

14. An apparatus comprising:

buffers to store data packets from a plurality of channels; and

a state machine coupled to the buffers to deskew the data packets while the data packets are stored in the buffers.

15. The apparatus of claim 14, wherein the state machine is adapted to hold the data packets in the buffers until a predetermined character is present in each of the buffers.

16. The apparatus of claim 15, further comprising a counter to count cycles occurring after receipt of a first data packet having the predetermined character.

17. The apparatus of claim 14, further comprising a plurality of state machines, each corresponding to one of the plurality of channels.

18. The apparatus of claim 14, wherein the data packets comprise InfiniBand data packets.

19. An article comprising a machine-readable storage medium containing instructions that if executed enable a system to:

receive a data sequence in a receiver having a plurality of lanes;

detect a predetermined character in the data sequence in a first lane; and

track a time period until the predetermined character is detected in the plurality of lanes.

20. The article of claim 19, further comprising instructions that if executed enable the system to reset the receiver if a predetermined number of cycles is exceeded before the predetermined character is detected in the plurality of lanes.

21. The article of claim 19, further comprising instructions that if executed enable the system to determine whether the data sequence is misaligned while the data sequence is maintained in buffers corresponding to the plurality of lanes.

22. A system comprising:

a switch fabric;

a plurality of buffers coupled to the switch fabric to receive data packets from a plurality of channels; and

a state machine coupled to the plurality of buffers to deskew the data packets while the data packets are received in the plurality of buffers.

23. The system of claim 22, further comprising a host channel adapter including the plurality of buffers.

24. The system of claim 23, wherein the host channel adapter further includes a counter to count cycles occurring after receipt of a first data packet having a predetermined character.

25. The system of claim 22, wherein the switch fabric comprises an InfiniBand switch fabric.